(1) The cited references are nonanalogous art.

Analogous art is all art that is either in the field of technology of the claimed invention or deals with the same problem solved by the claimed invention even though outside the field of technology. *In re Wood*, 599 F.2d 1032, 202 USPQ 171 (CCPA 1979).

Austin deals with sense amplifiers relating to static, low-power differential sense amplifiers as used in conventional memory cells such as in random access memories (RAMs). *See Austin, column one.* In contrast, Chung deals with a synapse MOS transistor that is useful in neural networks. *See Chung, column one.*

Further, Austin deals with the problem of power consumption in memory cells as noted in column one of Austin and reaffirmed in Austin's disclosure, for example, in column 8, lines 64-67: "[c]onsequently, power consumption according to the present invention is greatly reduced fro applications in which output read data sees a large capacitance."

In contrast, Chung deals with the problem of "the reduction of the number of connections between neurons, the multiplication of weights, and the summing of the weights at each node," *See, Chung column 1, lines 57-61.* A result of Chung's solution to his stated problem is a synapse MOS transistor that results in a reduced chip area, See, *Chung column 3, lines 34-36.* However, this size reduction is not the problem addressed by Chung.

Since Austin deals with conventional memories to address the problem of power consumption, and, in a different field addressing a different problem, Chung deals with synapse MOS transistor in neural networks to address the problem of the reduction of the number of connections between neurons, the Austin and Chung references are nonanalogous art, and their combination is not proper. Therefore, Applicant respectfully submits that all pending claims are patentable over Austin in view of Chung.

(2) There is no suggestion to combine Chung with Austin because combining them would render Austin unsatisfactory for its intended purpose.

Combining Chung with Austin by altering Austin to include the Chung synapse transistor would destroy the intended purpose of Austin to reduce power consumption. If a proposed modification would render the prior art invention being modified unsatisfactory for its intended

purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984); MPEP § 2143.01.

Austin deals with a pairs of NMOS transistors N5, N6 and N7,N8 coupled to PMOS transistors P5, P6, respectively, in which P5 and P6 are "substantially identically sized" to minimize switching current. *See, Austin, column 8, lines 10-13.*

In contrast, Chung deals with a synapse NMOS transistor to a synapse PMOS transistor, in which the synapse PMOS has gate electrodes twice that of the NMOS transistor *(See Chung column 3, lines 31-33)* and the synapse NMOS transistor has widths of varying lengths *(See Chung column 2, lines 21-24).* Thus, the PMOS transistors coupled to the NMOS in Chung are not identically sized.

Chung deals with a synapse transistor in which the transistors having common sources and drains have widths of varying lengths to provide various signal combinations for a neural network through using varying conductances through the synapse transistors. To combine the Chung reference with the Austin reference would result in a structure in which the PMOS transistors coupled to NMOS transistors would be sized substantially different as opposed to the PMOS transistors of Austin configured substantially identical to minimize power consumption. The Chung synapse transistor would not necessarily provide the intended result of Austin. Therefore, Application submits that there is no suggestion or motivation to make the proposed combination of Austin and Chung.

(3) There is no suggestion to combine Chung with Austin from the prior art and not from Applicant's specification .

The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991); MPEP § 2143. The Examiner must avoid hindsight. *In re Bond*, 910 F.2d 831, 834, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990).

Chung deals with NMOS and PMOS transistors, where the NMOS transistors have common sources and drains with multiple gates and the PMOS transistors have common sources and drains with multiple gates in which the number of gates for the NMOS transistors and the PMOS transistors are the same.

In contrast, Austin deals with a transistor pair in parallel, where the drain of each transistor is coupled to a source of a common PMOS transistor.

Applicant can not find any teaching or suggestion in the cited references for modifying the synapse NMOS/PMOS multiple gate structure of Chung to fit the sense amplifier structure of Austin. The Office Action reference to Chung's resulting synapse transistor having a reduced chip area ignores that the claimed combination does not have a reasonable expectation of success since Chung's multiple gated PMOS/NMOS synapse structure does not fit Austin's sense amplifier. Applicant only finds the use of a dual-gated MOS transistor in a sense amplifier in Applicant's disclosure. Therefore, Applicant respectfully submits that to avoid hindsight the Austin reference cannot be combined with the Chung reference.

Applicant can not find in Austin a teaching or suggestion of a dual-gated MOS as recited in the instant claims. Thus, Austin does not teach or suggest all the elements of each claim in which a dual-gated MOS is recited as part of an independent claim or depending from such an independent claim. Further, since Chung can not be properly combined with Austin, these discrepancies are not cured by Chung.

For the reasons stated above, Applicant submits that the pending claims are patentable over Austin in view of Chung.

Additional comments

With respect to claim 16, the Office Action states

> Austin's figure 1D shows all elements of the claims except for the sense amplifier is able to output a full output sense voltage in less than 10 nanoseconds (ns). However, it is well known in the art that the speed for the amplifier circuit dependent on the size of the transistors in the amplifier. Furthermore, Austin amplifier circuit having similar structure as Applicant amplifier circuit figure 2A. Therefore, Austin circuit is able to provide a full output of the sense voltage less than 10 nanoseconds depend on the size of the transistors in the amplifier. [I]t would have been obvious to one having ordinary skill in the art to modify the size of Austin amplifier circuit in order for the circuit is able to providing an output less than 10 nanoseconds because it is seen as a design choice.

Applicant can not find in Austin a teaching or suggestion regarding configuring a sense amplifier with respect to speed. Austin deals with a sense amplifier structured to reduce power consumption in which speed does not appear to be an issue.

Applicant requests that the Examiner provide a reference to show that a circuit "able to output a full output sense voltage in less than 10 nanoseconds (ns)," as recited by claim 16 is a member of a known group of devices or device characteristic from which a design choice can be made. A device having an element or characteristic that can be quantitatively recited does not make that element or its application to a claimed device a design choice subject to obviousness.

Further, the Office Action statement quoted above that "it would have been obvious to one having ordinary skill in the art to modify the size of Austin amplifier circuit in order for the circuit is able to providing an output less than 10 nanoseconds because it is seen as a design choice" is a conclusory statement for which no objective evidence has been provided. Since no reference has bee provided for this statement, Applicant requests the Examiner to provide a reference that describes such an element. Absent a reference, it appears that the Examiner is using personal knowledge, so the Examiner is respectfully requested to submit an affidavit as required by 37 C.F.R. § 1.104(d)(2).

For the various reasons stated above, Applicant requests withdrawal of these rejections to claims 10-11, 13-14, 16-18, 20-24, 26-27, 29-38, 44, and 45, and reconsideration and allowance of these claims.

Second §103Rejection of the Claims

Claim 15 was rejected under 35 USC § 103(a) as being unpatentable over Austin (U.S. 5,982,690) in view of Chung (U.S. 5,442,209) and Ang et. al. (5,942,918). Applicant traverses these grounds for rejection.

Applicant does not admit that the Austin patent is prior art to the present invention and reserves the right to swear behind this patent at a later date. Nevertheless, Applicant also submits that the Austin patent is distinguishable from the present invention.

Claim 15 is dependent on claim 10, where claim 10 recites "a dual-gated metal-oxide semiconducting field effect transistor." Applicant can not find in Austin a teaching or suggestion of a dual-gated metal-oxide semiconducting field effect transistor as recited in claims 10 and 15. As previously discussed, combining Austin with Chung is improper, and, therefore the deficiencies of Austin are not cured.

The Office Action applies Ang et al. (hereafter Ang) stating "Ang et al.'s amplifier circuit operable with a supply voltage less than 1 volts (column 1, lines 50-55)." Ang also does not cure the deficiencies of Austin. Thus, since Chung is not properly combined with Austin, Austin in view of Chung and Ang does not teach or suggest all the elements of claim 15.

Applicant requests withdrawal of this rejection to claim 15, reconsideration and allowance of claim 15.

Third §103Rejection of the Claims

Claims 28 and 40-43 were rejected under 35 USC § 103(a) as being unpatentable over Kaneko et al. (U.S. 6,069,828) in view of Austin (U.S. 5,982,690) and Chung (U.S. 5,442,209). Applicant traverses these grounds for rejection.

Applicant does not admit that the Austin patent is prior art to the present invention and reserves the right to swear behind this patent at a later date. Nevertheless, Applicant also submits that the Austin patent is distinguishable from the present invention.

Claim 28 is dependent on claim 23, where claim 23 recites "a dual-gated metal oxide semiconductor (NMOS) transistor." Applicant can not find in Austin a teaching or suggestion of a dual-gated metal-oxide semiconductor NMOS transistor as recited in claims 23 and 28. As previously discussed, combining Austin with Chung is improper, and, therefore the deficiencies of Austin are not cured.

The Office Action applies Kaneko et al. (hereafter Kaneko) noting that Kaneko "shows all elements of the claim except for the detail of the sense amplifier." Therefore, Kaneko also does not cure the deficiencies of Austin. Thus, since Chung is not properly combined with Austin, Austin in view of Chung and Kaneko does not teach or suggest all the elements of claim 28.

Claim 40 recites "equilibrating a first and second bit line, wherein the first bit line is coupled to a first gate of a dual-gate transistor." As stated above, Kaneko does not cure the deficiencies of Austin with respect to a dual-gate transistor, and combining Austin with Chung is improper. Therefore, Kaneko does not cure the deficiencies of Austin.

Additional comments

With respect to claim 42, the Office Action states

> Austin's figure 1D shows all elements of the claims except for the sense amplifier is able to output a full output sense voltage in less than 10 nanoseconds (ns). However, it is also seen as a design choice for designing the output speed of the sense amplifier to be able to output a full sense voltage in less than 10 nanoseconds (ns) dependent upon particular environment of use to ensure optimum performance.

The discussion with respect to claim 16 above is applicable to claim 42.

Claims 41-43 are dependent on claim 40 and are patentable over Kaneko in view of Austin and Chung for the reasons stated above plus the elements of these claims.

Applicant respectively requests withdrawal of these rejections of claims 28 and 40-43, and reconsideration and allowance of these claims.

Assertion of Pertinence

Applicant need not respond to the assertion of pertinence stated for the references cited but not relied upon by the Office Action since these references are not made part of the rejections in this Office Action. Applicant is expressly not admitting to this assertion and reserves the right to address the assertion should it form part of future rejections.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (612-371-2157) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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Date 20 February 2003 By David R. Cochran

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 20th day of February, 2003.

Amy Moriarty
Name

Signature